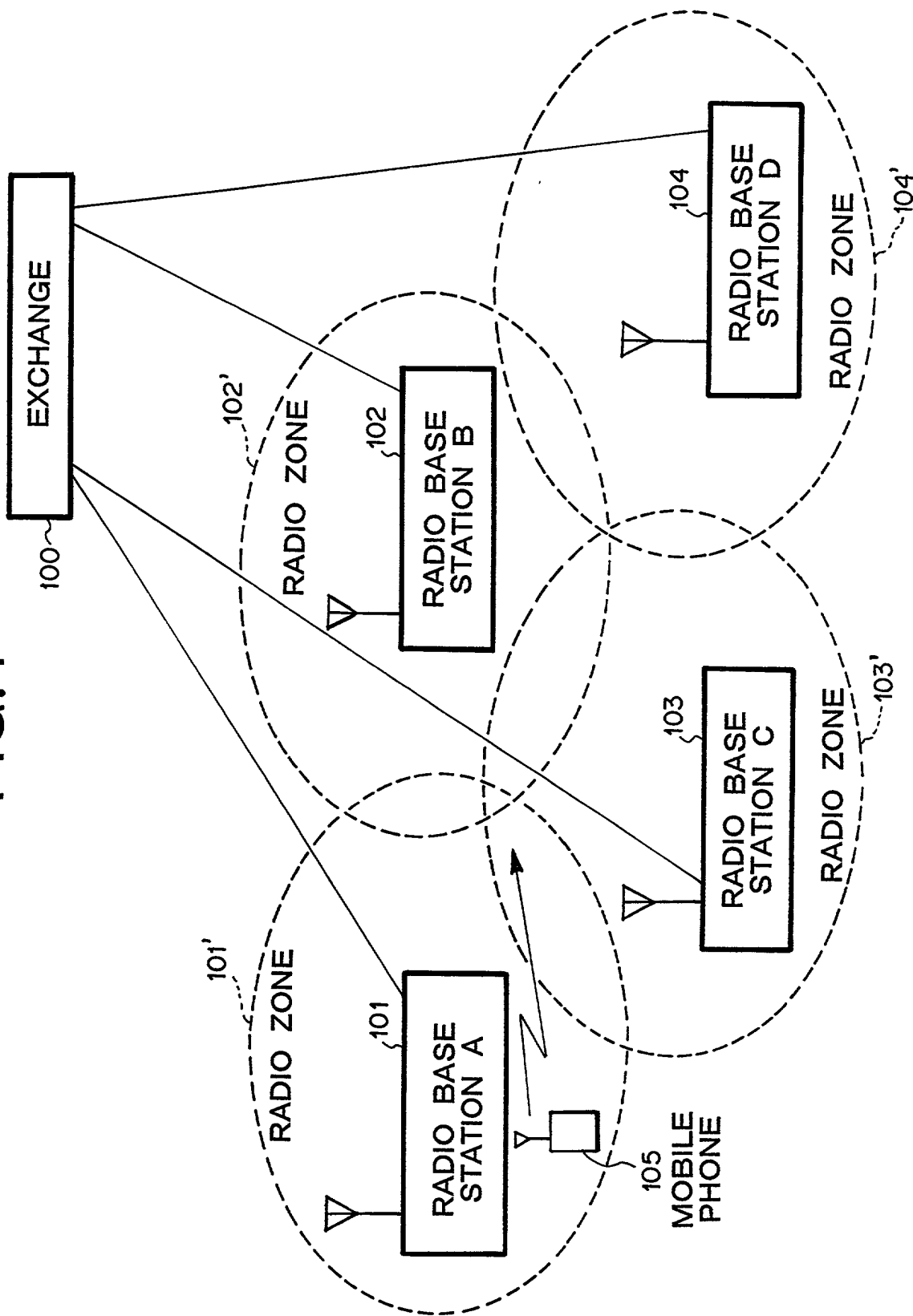


FIG. 1



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FIG.2A

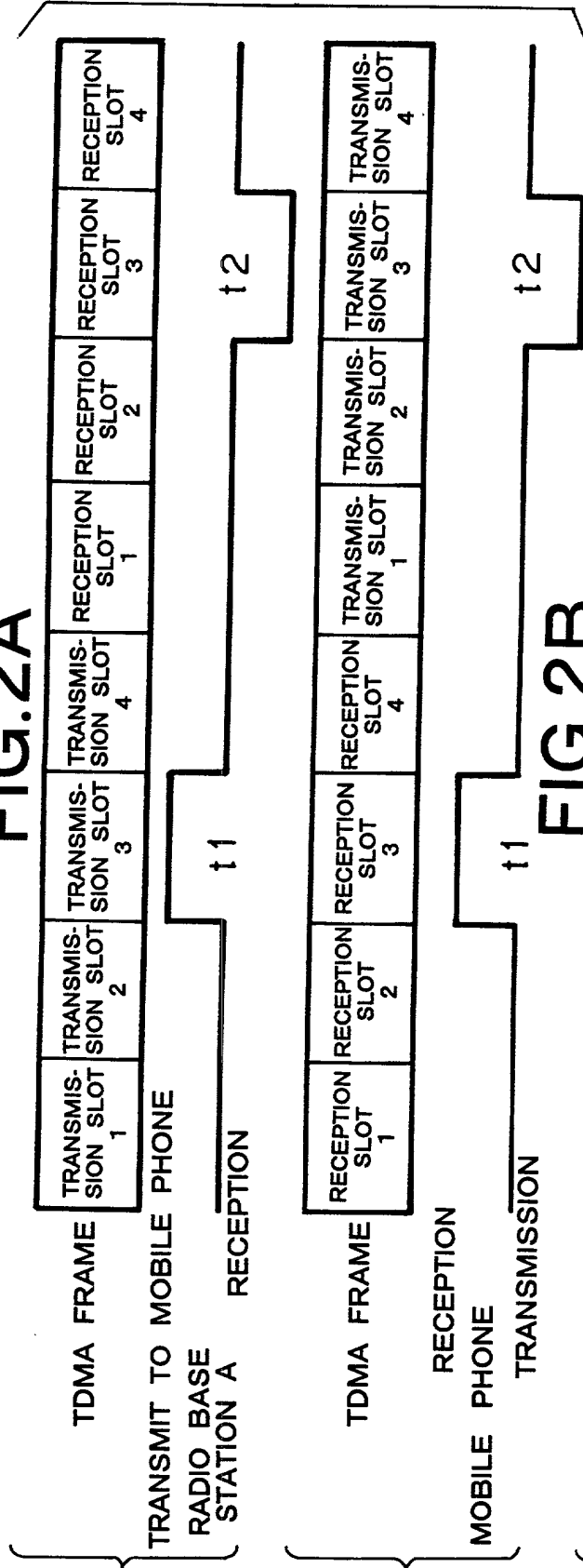
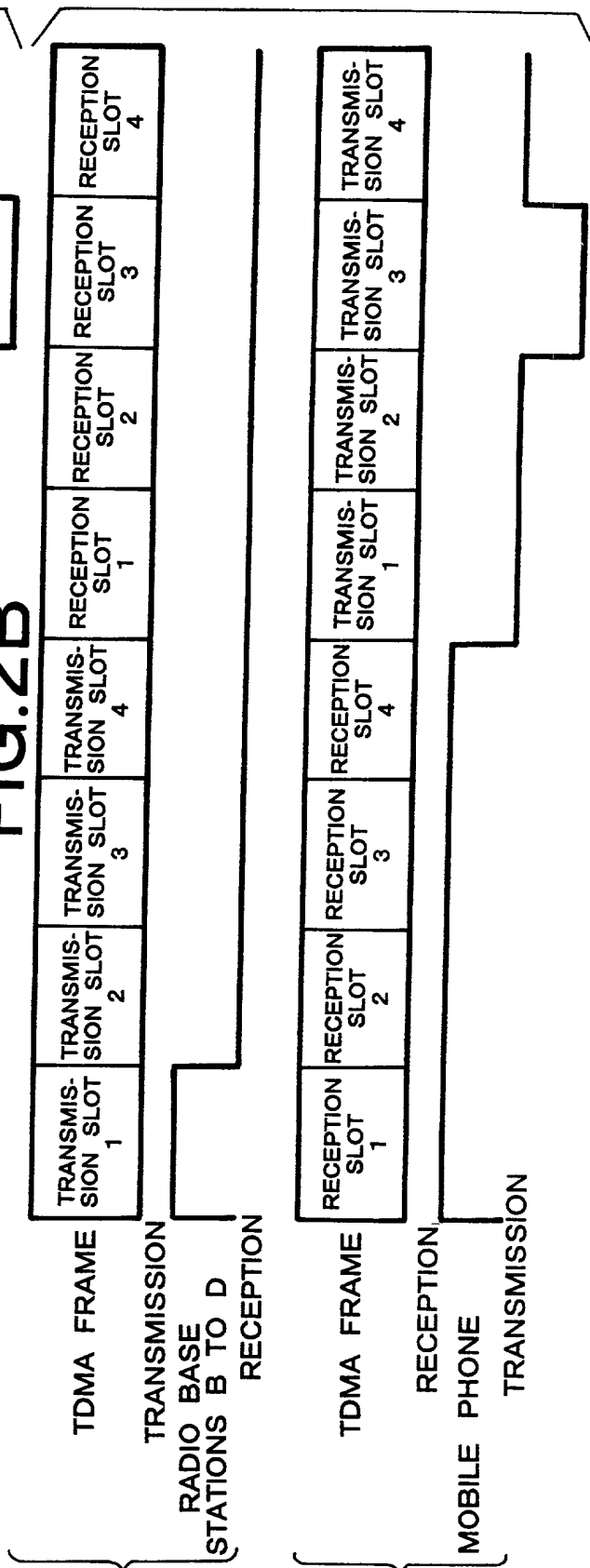


FIG.2B



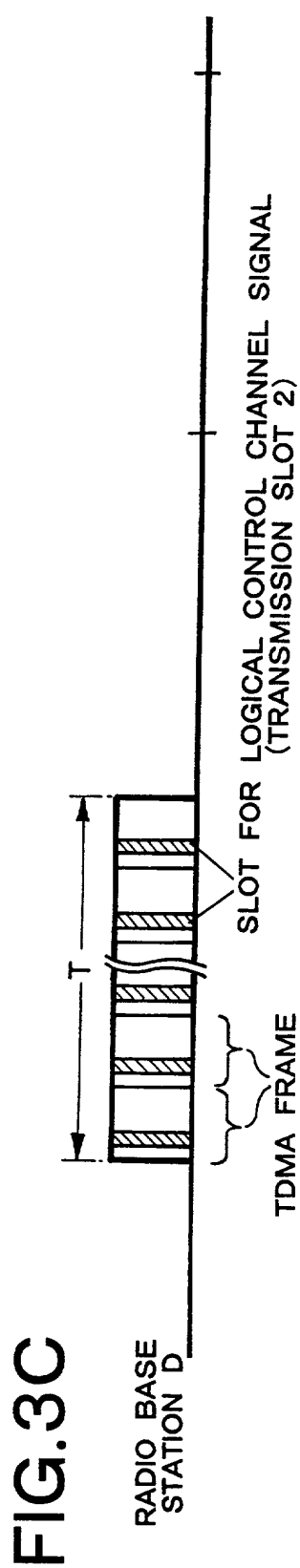
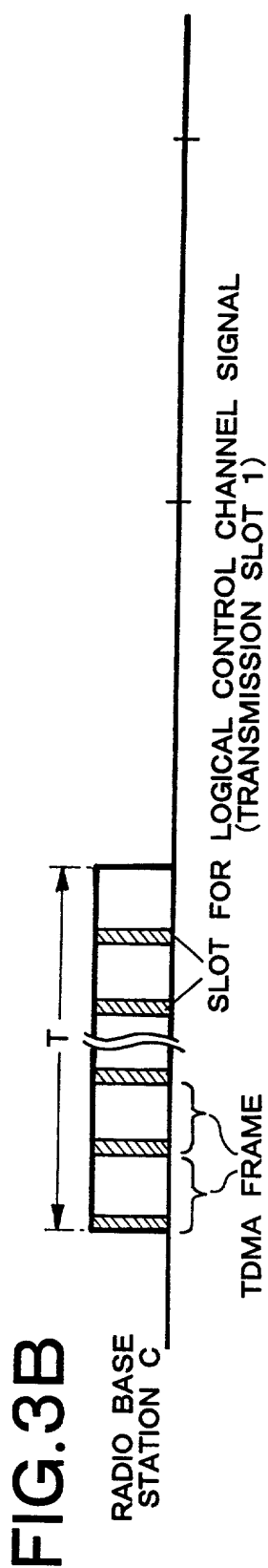
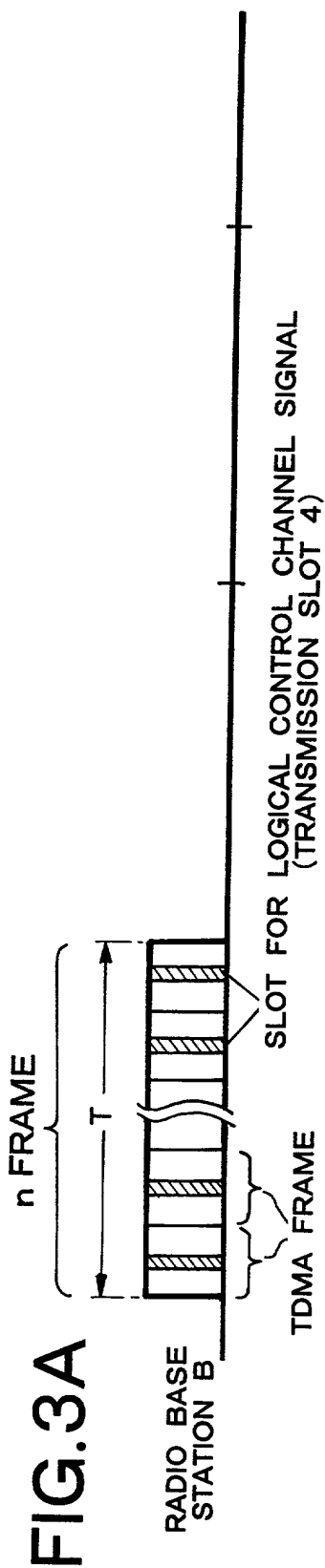


FIG. 4

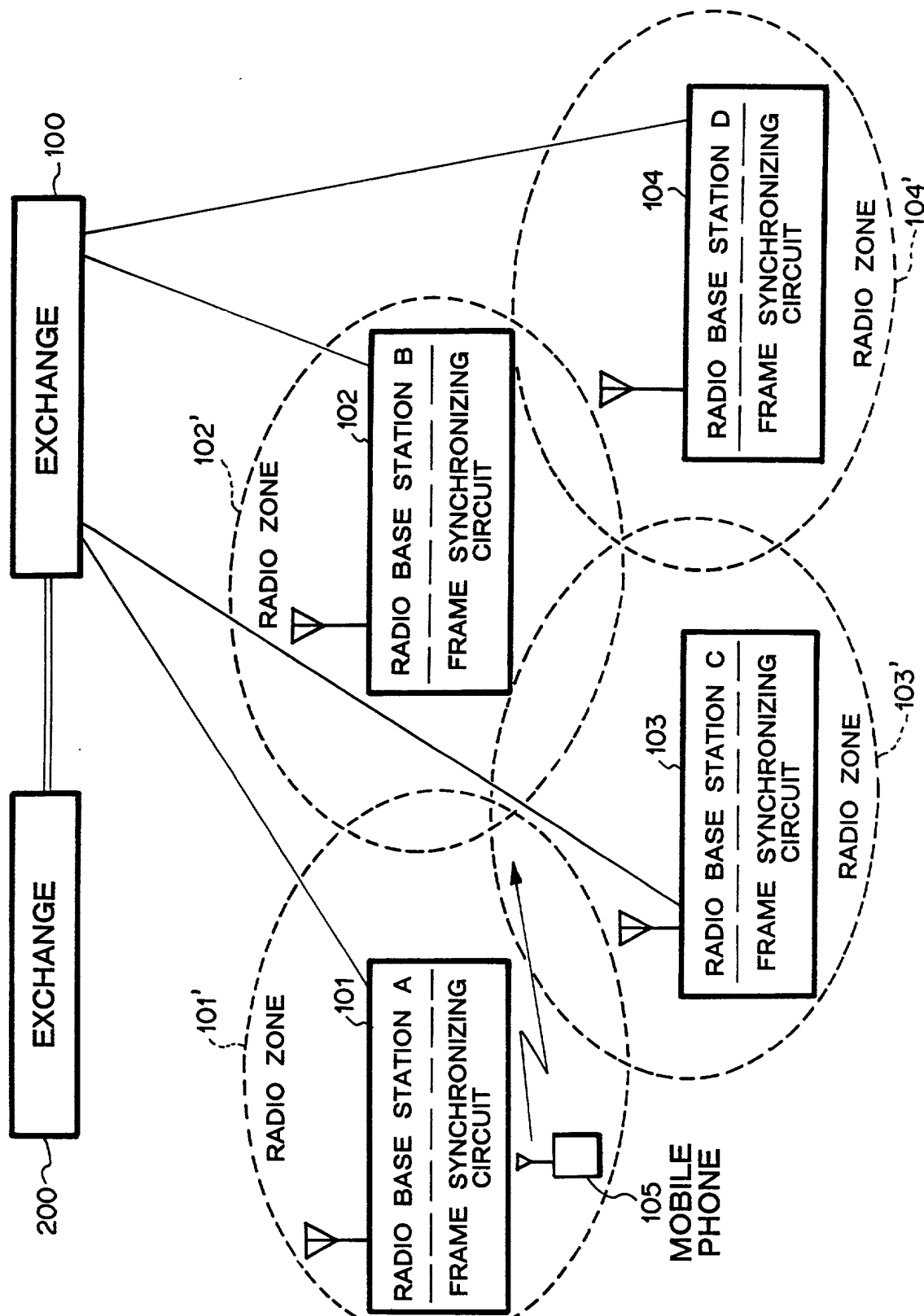
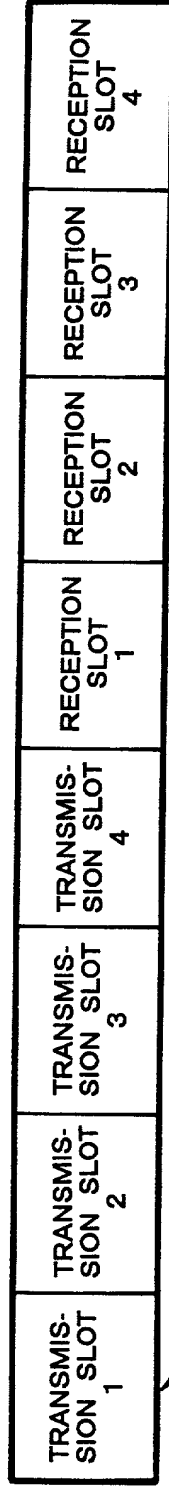
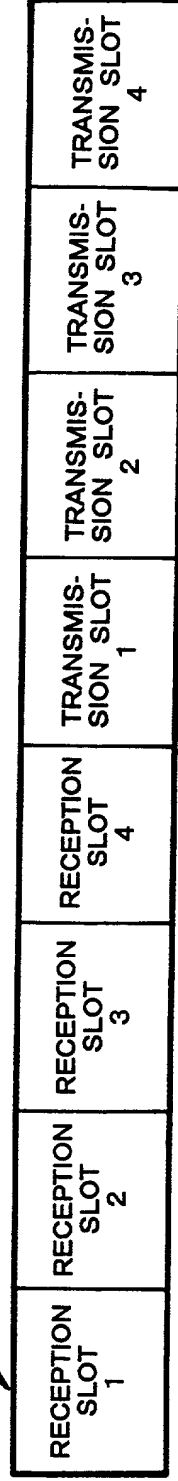


FIG. 5A



SLOT FOR LOGICAL CONTROL CHANNEL SIGNAL

FIG. 5B



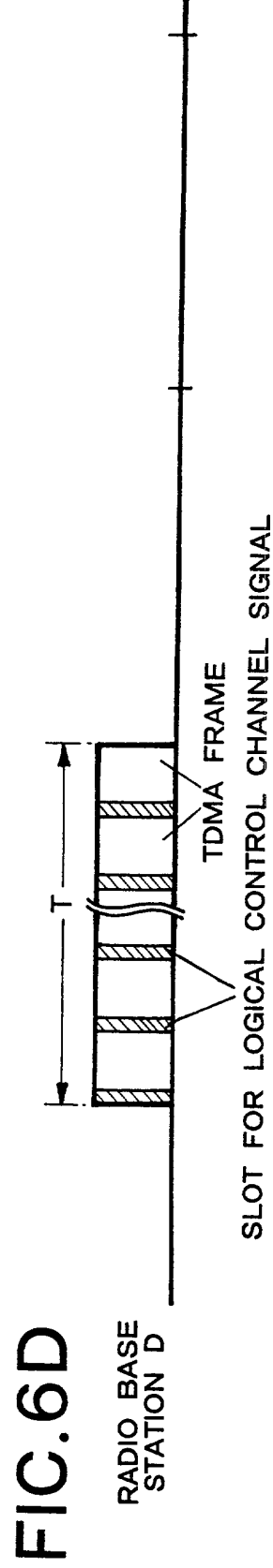
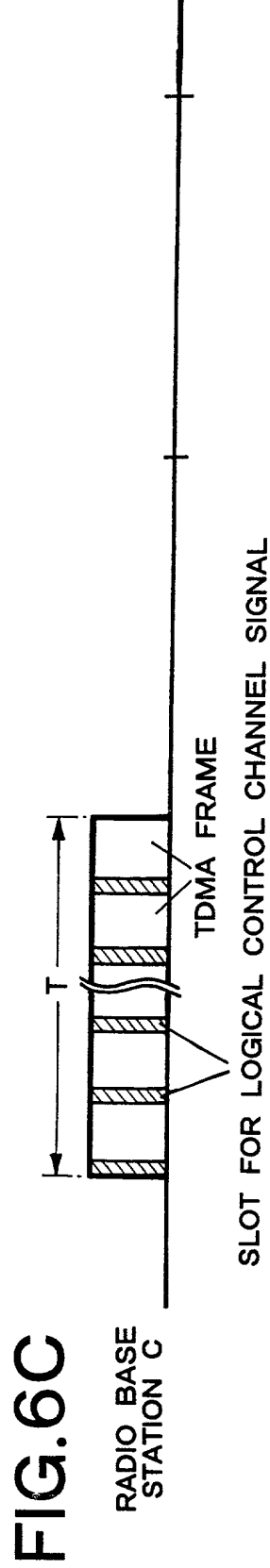
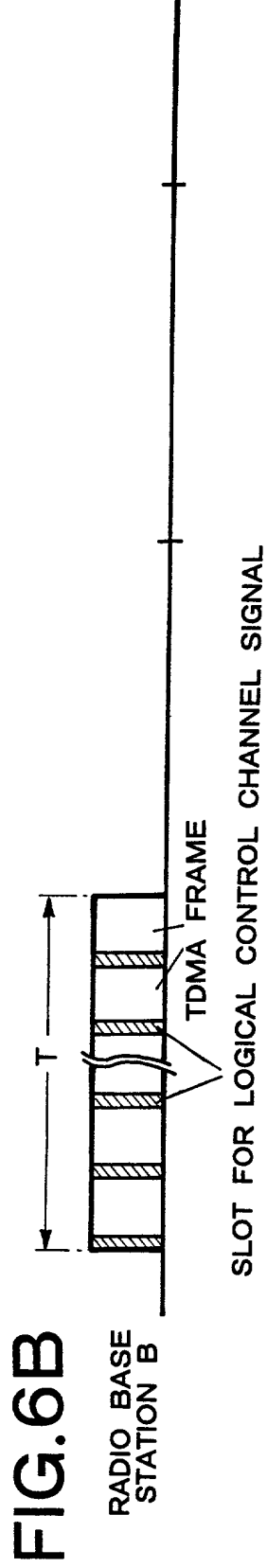
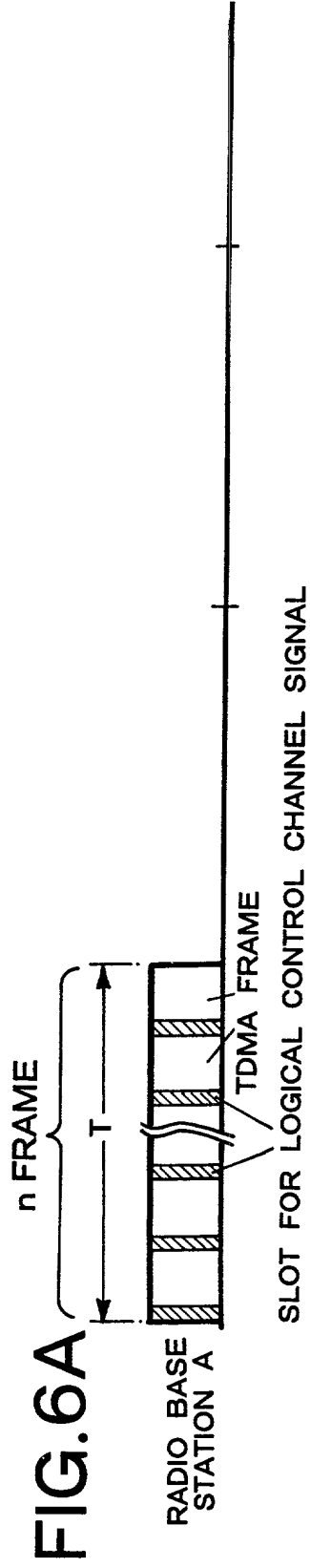


FIG. 7A

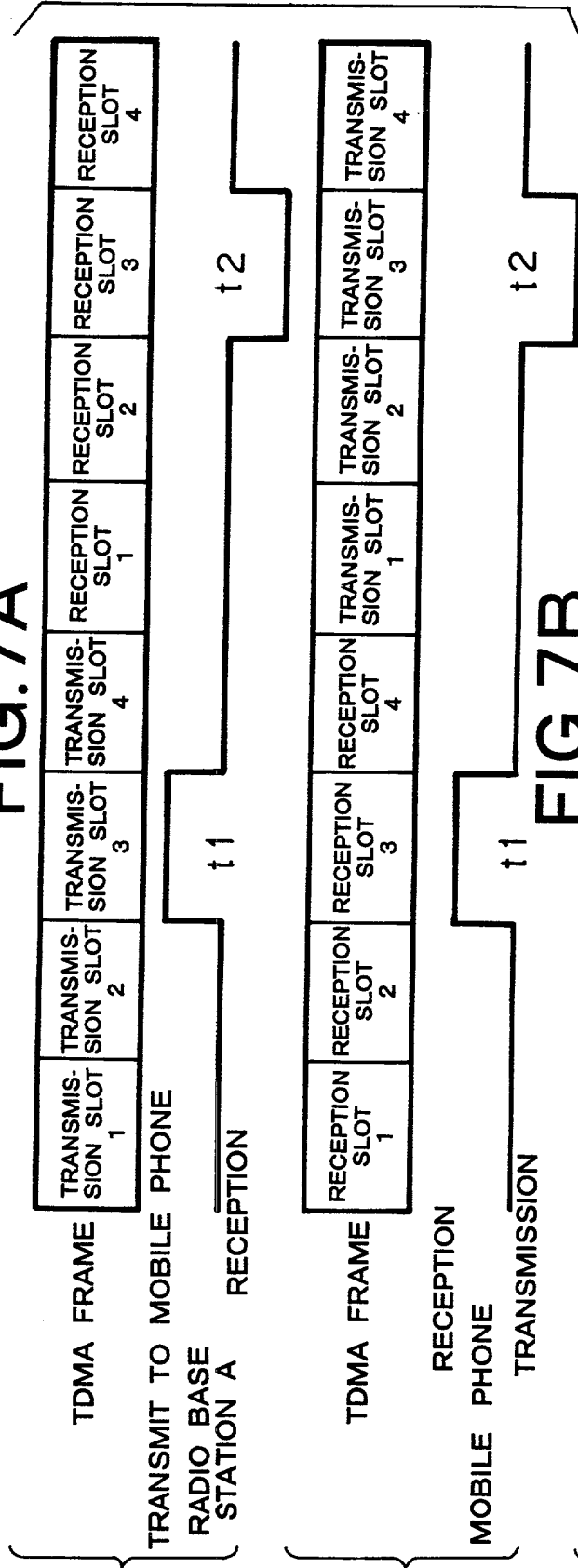


FIG. 7B

